Tentative

CM100DU-24NFH

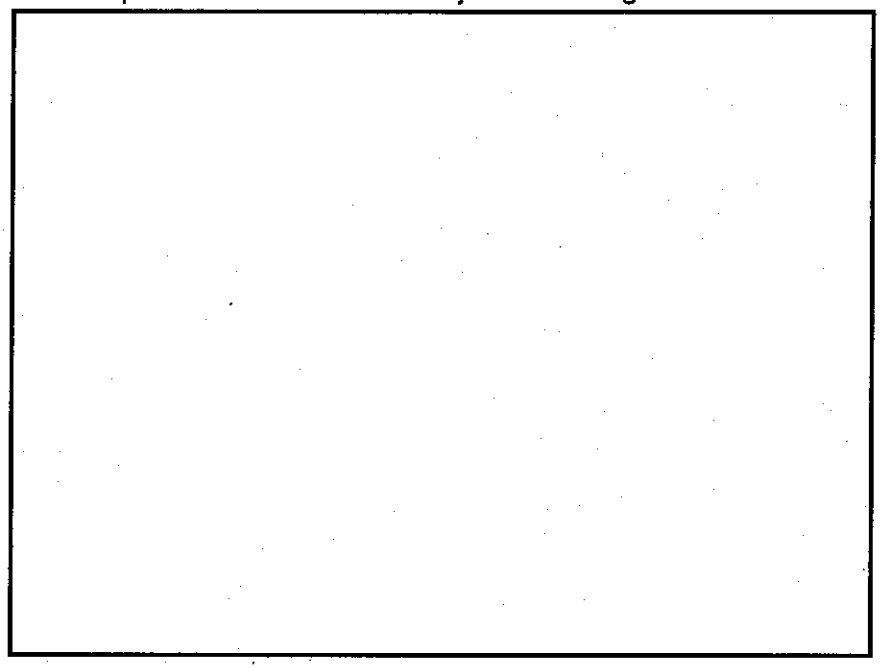
Pre.	M.Koura	Rev	A	M. Koura
Apr.	M.Tabata 2-Nov.'02			M. Tabata 9-Apr.-'03

HIGH POWER SWITCHING USE

Notice : This is not a final specification. Some parametric limits are subject to change.

CM100DU-24NFH

- Ic ····· 100A
- V_{CES} ····· 1200V
- Insulated Type
- 2-elements in a pack



APPLICATION

High frequency switching use (30kHz to 60kHz).
Gradient amplifier,Induction heating,power supply,etc.

ABSOLUTE MAXIMUM RATINGS (T_j = 25 °C)

Symbol	Item	Conditions	Ratings	Units
V_{CES}	Collector-emitter voltage	G-E Short	1200	V
V_{GES}	Gate-emitter voltage	C-E Short	±20	V
I_C	Collector current	Tc= 25 °C	100	A
I_{CM}		Pulse ②	200	
I_E ①	Emitter current	Tc= 25 °C	100	A
I_{EM} ①		Pulse ②	200	
Pc ③	Maximum collector dissipation	Tc= 25 °C	560	W
Pc ③	Maximum collector dissipation	Tc' = 25 °C*4	730	W
Tj	Junction temperature		−40~+150	°C
Tstg	Storage temperature		−40~+125	°C
Viso	Isolation voltage	Main terminal to base plate,AC 1 min.	2500	V
—	Torque strength	Main terminal M5	2.5 ~ 3.5	N·m
—	Torque strength	Mounting holes M6	3.5 ~ 4.5	N·m
—	Weight	Typical value	310	g

A

ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

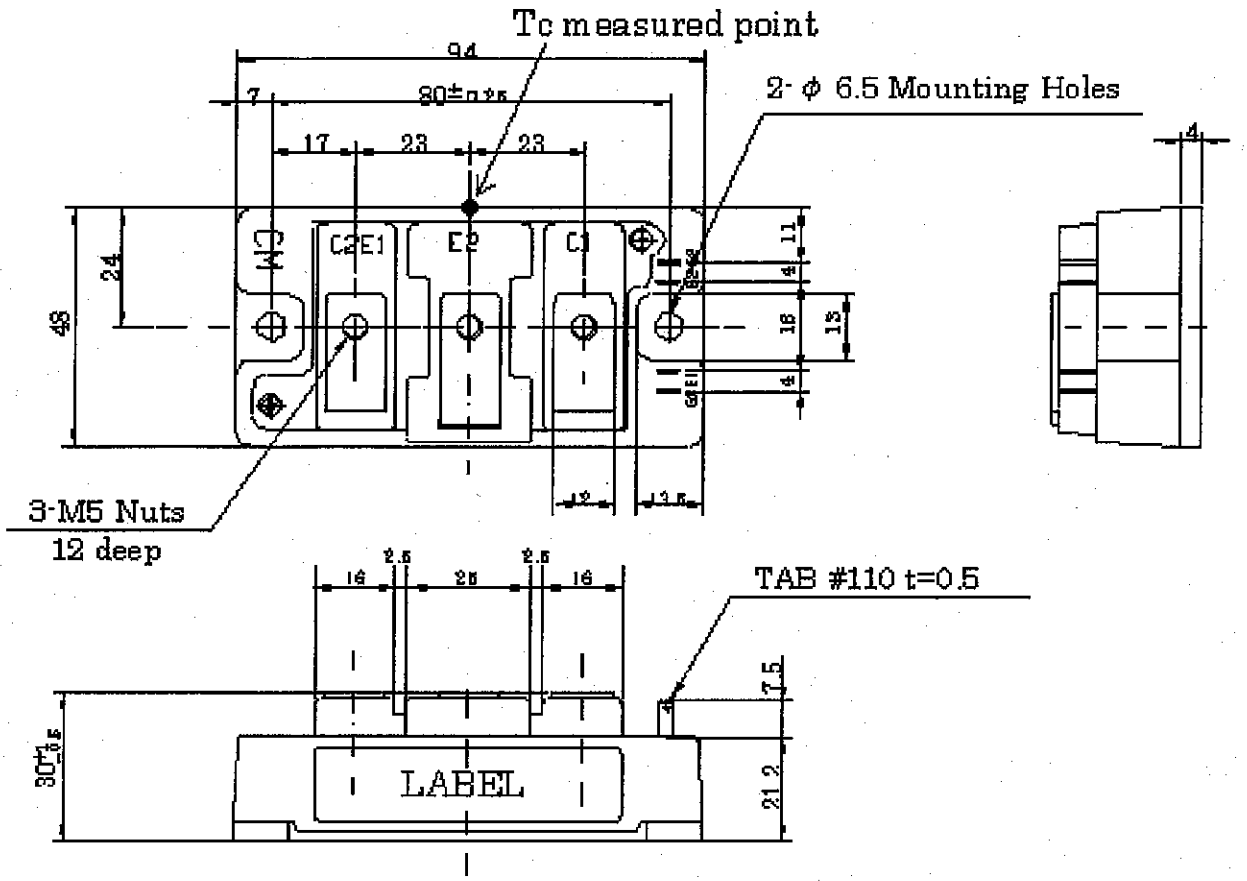
Symbol	Item	Conditions		Min.	Typ.	Max.	Units	
I_{CES}	Collector cutoff current	$V_{CE}=V_{CES}, V_{GE}$= 0V		–	–	1	mA	
$V_{GE(th)}$	Gate-emitter threshold voltage	I_C=10mA, V_{CE}= 10V		5	6	7	V	
I_{GES}	Gate leakage current	$V_{GE}=V_{GES}$, V_{CE}= 0V		–	–	0.5	μA	
$V_{CE(sat)}$	Collector to emitter saturation voltage ④	T_j= 25 °C	I_C = 100A	–	5.0	6.5	V	A
		T_j= 125 °C	V_{GE}= 15V	–	5.0	–		
Cies	Input capacitance	V_{CE}= 10V		–	–	16	nF	
Coes	Output capacitance	V_{GE}= 0V		–	–	1.3		
Cres	Reverse transfer capacitance			–	–	0.3		
Q_G	Total gate charge	V_{CC}=600V, Ic=100A, V_{GE}=15V		–	450	–	nC	
td(on)	Turn-on delay time	V_{CC}=600V, Ic=100A		–	–	100	ns	
tr	Turn-on rise time	$V_{GE1}=V_{GE2}$=15V		–	–	50		
td(off)	Turn-off delay time	R_G=3.1Ω, Inductive load		–	–	250		A
tf	Turn-off fall time	switching operation		–	–	150		
trr ①	Reverse recovery time	I_E=100A		–	–	150		
Qrr ①	Reverse recovery charge			–	5.0	–	μC	
V_{EC} ①	Emitter-collector voltage	I_E=100A, V_{GE}= 0V		–	–	3.5	V	
Rth(j-c)Q	Thermal resistance	IGBT part (1/2 module)		–	–	0.22	°C/W	
Rth(j-c)R		FWDi part(1/2 module)		–	–	0.47		A
Rth(c-f)	Contact thermal resistance	Case to fin, Thermal compound Applied (1/2module) *2		–	0.07	–		
Rth(j-c')Q	Thermal resistance *4	IGBT part (1/2 module)		–	–	0.17*3		A
Rth(j-c')R		FWDi part(1/2 module)		–	–	0.29*3		
RG	External gate resistance			3.1	–	31	Ω	

*1: Tc measured point is shown in page OUTLINE DRAWING.
*2: Typical value is measured by using Shin-etsu Silicone "G-746".
*3: If you use this value , Rth(f-a) should be measured just under the chips.
*4: Tc' measured point is just under the chips.

① I_E, V_{EC}, trr, Qrr & die/dt represent characteristics of the anti-parallel, emitter to collector free-wheel diode (FWDi).
② Pulse width and repetition rate should be such that the device junction temp.(T_j) dose not exceed Tjmax rating.
③ Junction temperature (T_j) should not increase beyond 150°C.
④ Pulse width and repetition rate should be such as to cause neglible temperature rise.
⑤ No short circuit capability is designed.

OUTLINE DRAWING

Dimensions in mm



CIRCUIT DIAGRAM